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## **INNOVATIVE IMMUNITY TO ELECTROSTATIC DISCHARGE TESTING METHOD USING THE VERY-FAST TRANSMISSION LINE PULSE CONCEPT**

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### **Abstract**

The transmission line pulse (TLP) method it is one of the most advantageous electrostatic discharge (ESD) testing method for semiconductor devices. A new factual approach is developed in this paper which is based on TLP method. The new method is named “very-fast transmission line pulse” (VF-TLP), having as principal characteristics the very short pulse width and small rise time. The appropriate device under test (DUT) is a gate-grounded (GG) NMOS transistor. The testing signal was applied on drain electrode, while the gate, source and substrate electrodes are connected to the ground. The obtained results are used to describe the parameters of the MOSFET transistors, having also relevance upon environment protection, due to the performed tests and to their inherent rejections. All the tests made or all the devices used in simulations can pollute the surrounding environment.

*Key words:* electrostatic discharges, EMC pollution, GGNMOS, line pulse, semiconductor device, very-fast transmission,

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